

CHARLES B. GORDON  
THOMAS P. SCHILLES  
DAVID B. DEIOMA  
JOSEPH J. CORSO  
HOWARD G. SHIMOLA  
JEFFREY J. SOPKO  
JOHN P. MURTAUGH  
JAMES M. MOORE  
MICHAEL W. GARVEY  
RICHARD A. SHARPE  
RONALD M. KACHMARIK  
PAUL A. SERBINOWSKI



09 954691  
**PEARNE & GORDON LLP**

ATTORNEYS AT LAW  
1801 EAST 9th STREET  
SUITE 1200

CLEVELAND, OHIO 44114-3108

TEL: (216) 579-1700 FAX: (216) 579-6073

EMAIL: ip@pearnegordon.com

COFC  
STEPHEN S. WENTSLE  
BRIAN G. BEMBENICK  
AARON A. FISHMAN  
ROBERT F. BODI  
SUZANNE B. GAGNON  
UNA L. LAURICIA  
STEVEN J. SOLOMON  
GREGORY D. FERNENGEL  
OF COUNSEL  
LOWELL L. HEINKE  
THADDEUS A. ZALENSKI  
PATENT, TRADEMARK,  
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September 23, 2004

Mail Stop Certificate of Corrections Branch  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Re: U.S. Patent No.: 6,787,876  
Issued: September 7, 2004  
Inventor: Martin Clive Wilson  
Our Docket: 33908

**Certificate**  
**OCT 04 2004**  
**of Correction**

Sir:

A Certificate of Correction under 35 U.S.C. 254 is hereby requested to correct Patent Office printing errors in the above-identified patent. Enclosed herewith is a proposed Certificate of Correction (Form No. PTO-1050) for consideration along with appropriate documentation supporting the request for correction.

It is requested that the Certificate of Correction be completed and mailed at an early date to the undersigned attorney of record. The proposed corrections are obvious ones and do not in any way change the sense of the application.

We understand that a check is not required since the errors were on the part of the Patent and Trademark Office in printing the patent.

Very truly yours,

Jeffrey J. Sopko, Reg. No. 27676

JJS:vlh  
Enclosures

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date indicated below.

Jeffrey J. Sopko

Name of Attorney for Applicant(s)

September 23, 2004

Date

Signature of Attorney

OCT 05 2004

**UNITED STATES PATENT AND TRADEMARK OFFICE  
CERTIFICATE OF CORRECTION**

PATENT NO. : 6,787,876 B2  
DATED : September 7, 2004  
INVENTOR(S) : Martin Clive Wilson

PAGE 1 OF 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 4

Line 43, after "from" please delete "1" and insert therefor - - 3 - -.

MAILING ADDRESS OF SENDER: Jeffrey J. Sopko  
Pearne & Gordon LLP  
1801 East 9th Street  
Suite 1200  
Cleveland, Ohio 44114-3108

PATENT NO. 6,787,876 B2

No. of additional copies

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OCT 05 2004

1           **Claim 3    (Original):**    A semiconductor device is  
2       claimed in claim 2, wherein said distance lies within the  
3       range of from 3  $\mu$ m to 5  $\mu$ m.

1           **Claim 4    (Original):**    A semiconductor device as  
2       claimed in any one of claims 1 to 3, wherein there are two  
3       trenches, each of which has the features defined in  
4       claim 1, and wherein an active device is formed in the  
5       semiconductor material layer between the two trenches.

1           **Claim 5    (Currently amended):** A semiconductor device  
2       as claimed in any one of claims 1 to ~~[[4]]~~ 3, wherein there  
3       are a plurality of trenches, each of which has the features  
4       defined in claim 1, and wherein a respective active device  
5       is formed in the semiconductor material layer between each  
6       pair of adjacent trenches.

1           **Claim 6    (Currently amended):** A semiconductor device  
2       as claimed in any one of claims 1 to ~~[[5]]~~ 3, wherein the  
3       semiconductor material layer is a silicon layer.

1           **Claim 7    (Original):**    A semiconductor device as  
2       claimed in claim 6, wherein the silicon layer is of single  
3       crystal formation.